



04/13 Add DC-IN Cable DC301008200 (45@)

07/21 Add DAZ P/N and other small board PCB P/N

# Compal Confidential

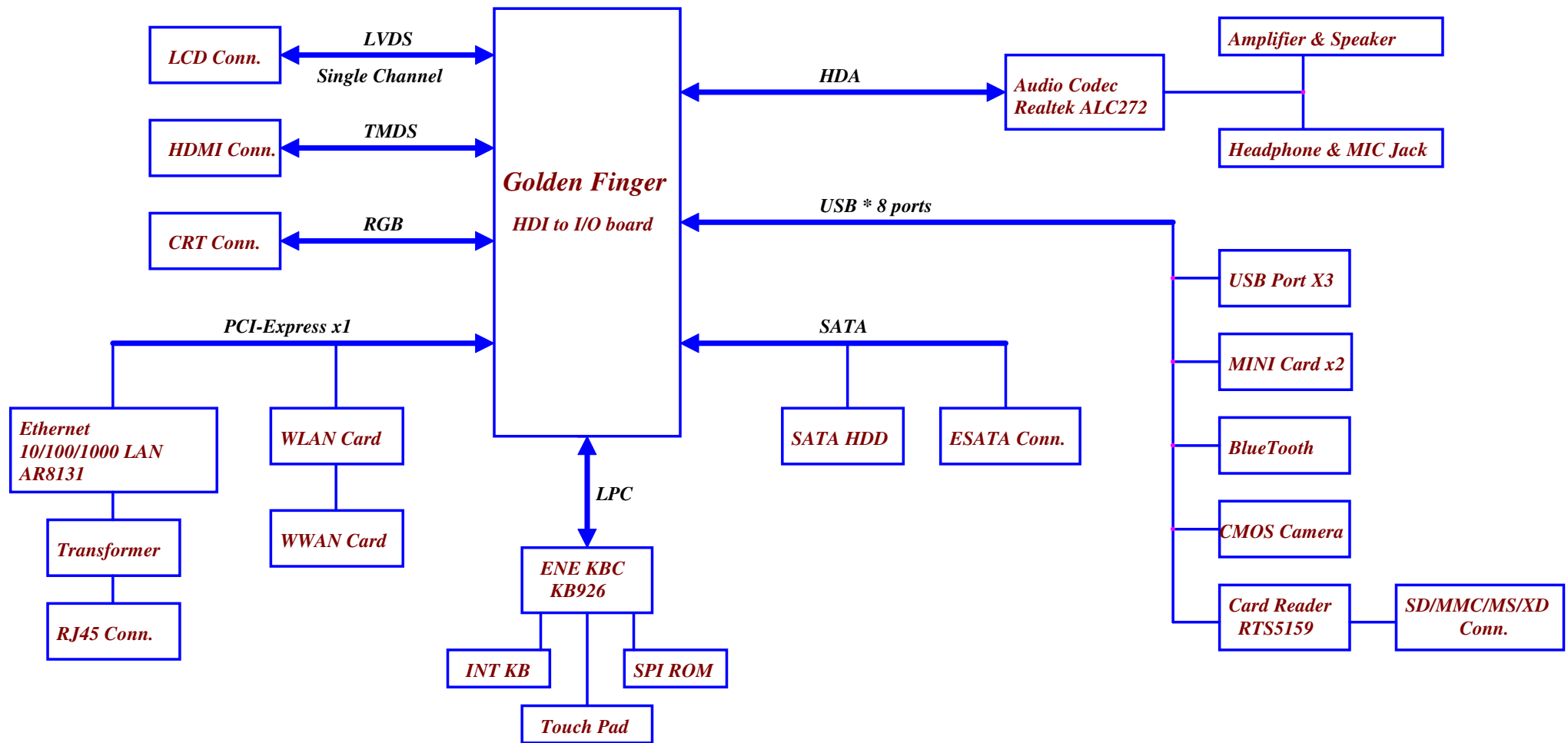
## NTUC0 LA-5501P Schematics Document

Intel Penryn uFCBGA with Intel Cantiga GS40+ICH9M SFF

### SFF ULV I/O Board

2009-07-30

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				Date	Thursday, July 30, 2009
				Sheet	1 of 24
				Rev	1.0



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				Size	Document Number	Rev
				Custom	NTUC0 IO/B LA-5501P Schematic	1.0
Date: Thursday, July 30, 2009				Sheet	2	of 24

### Symbol Note :



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build

CONN@ : means ME part.

45@ : means install after SMT.

### I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

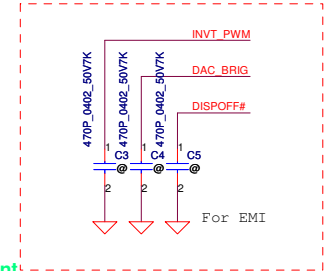
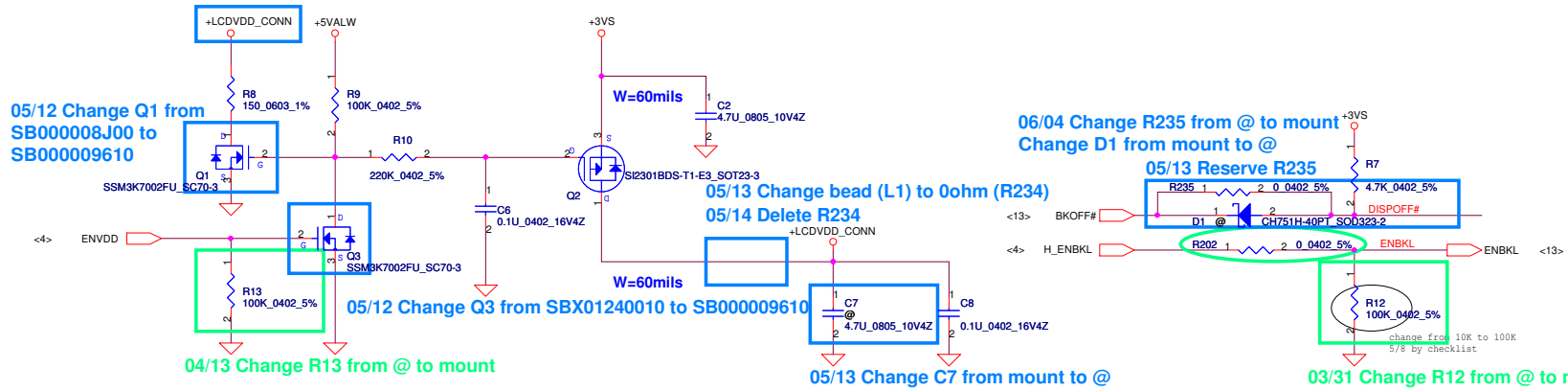
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CLK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CLK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CLK_CLK1 SMB_CLK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

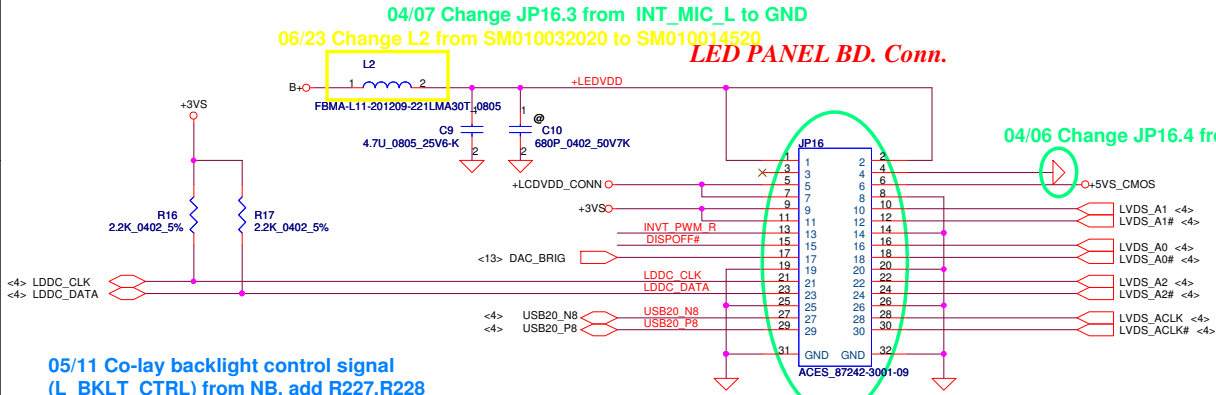
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				Date: Tuesday, July 21, 2009	Sheet 3 of 24



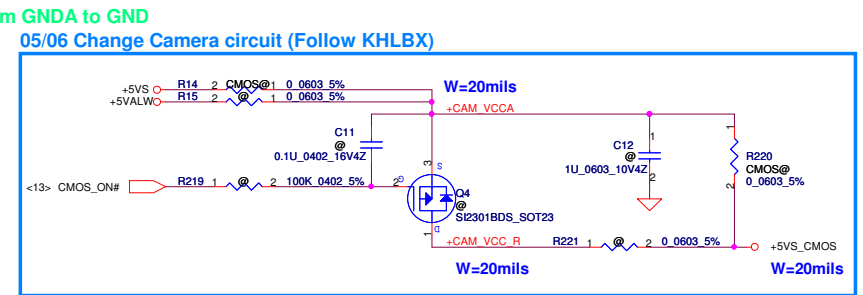
## LCD POWER CIRCUIT



**LED PANEL BD. Conn.**



## CMOS Camera



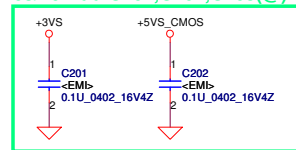
05/11 Co-lay backlight control signal (L\_BKLT\_CTRL) from NB, add R227,R228



06/04 Change R227 from mount to @  
Change R228 from @ to mount

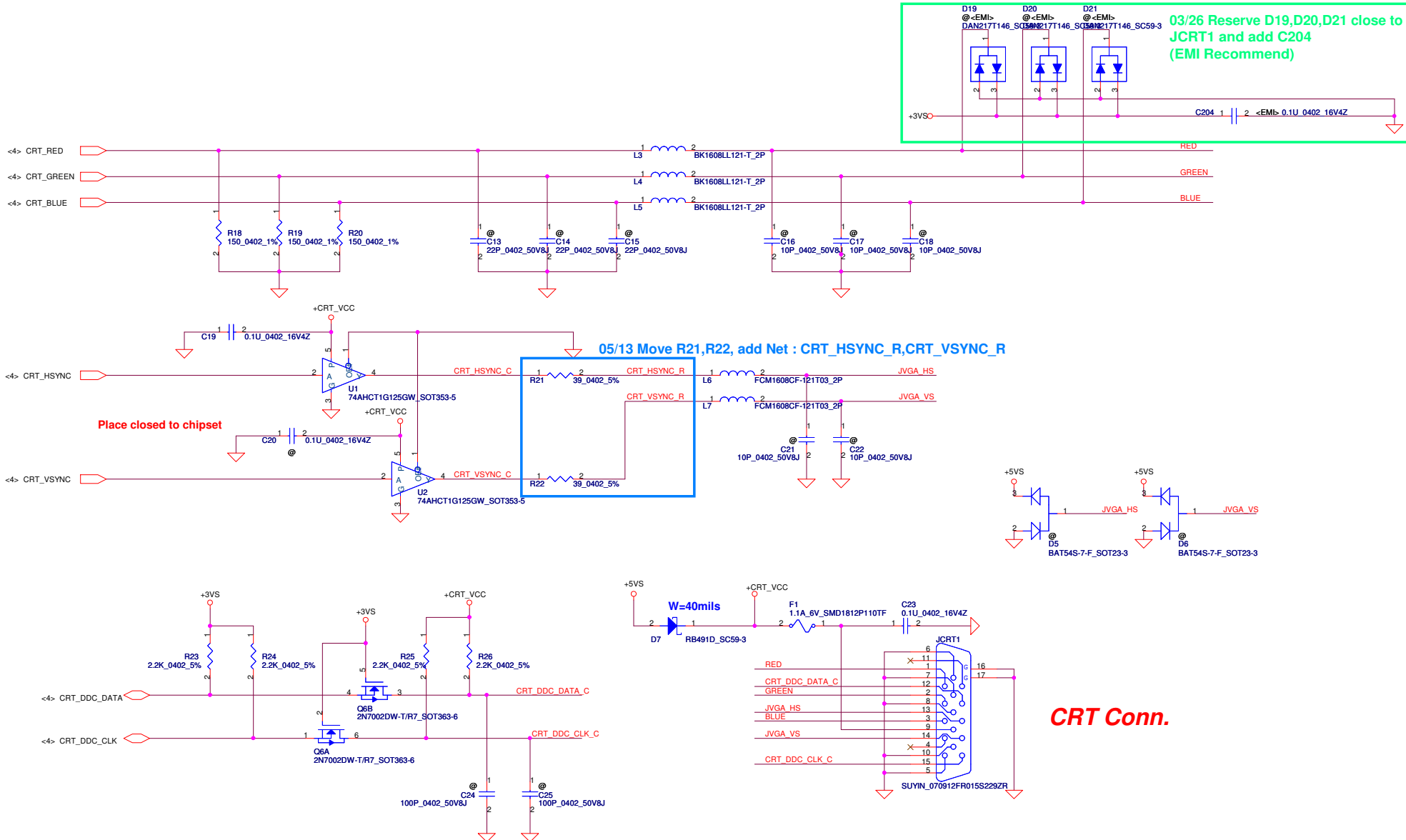
03/24 Change JP16 to right angle conn.

03/26 Add C201,C202,C203(@) close to JP16 (EMI Recommend)



**04/06 Delete C203 for layout**

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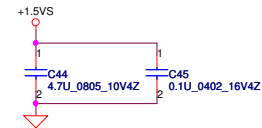
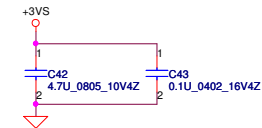
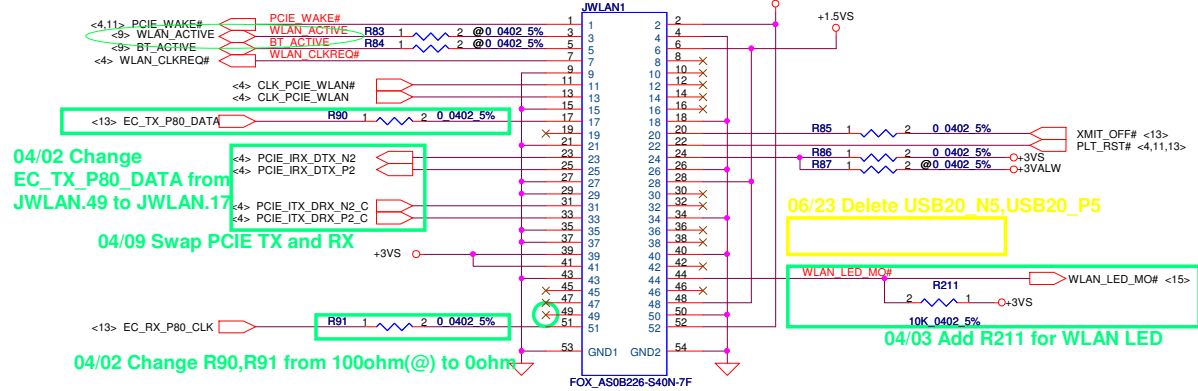


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								Rev			
								1.0			
								Date: Thursday, July 30, 2009			
								Sheet 6 of 24			

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				Custom	
				Date:	Thursday, July 30, 2009

## Mini-Express Card (Slot 1-WLAN) 4mm High

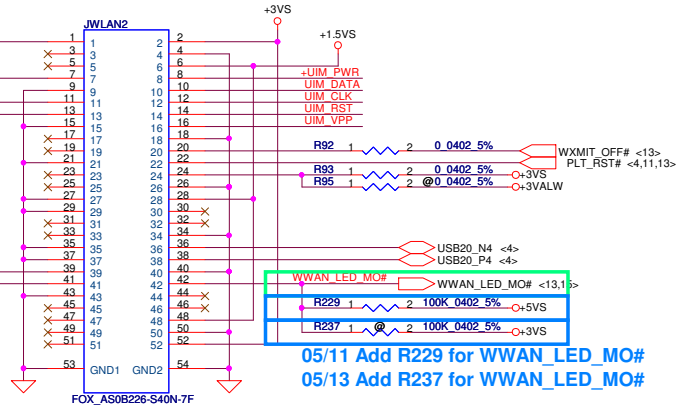
04/02 Swap Net : WLAN\_ACTIVE and BT\_ACTIVE (Follow JHXXX)



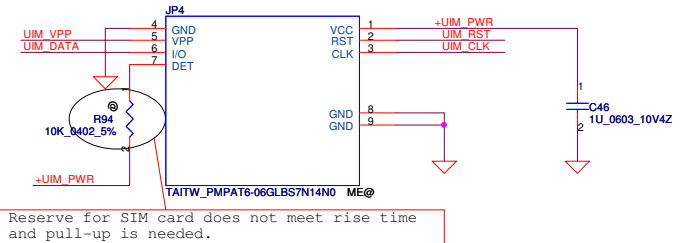
## Mini-Express Card (Slot 2-WWAN) 4mm High

04/09 Swap PCIE TX and RX

06/23 Delete PCIE\_IRX\_DTX\_N4,PCIE\_IRX\_DTX\_P4  
PCIE\_ITX\_DRX\_N4\_C,PCIE\_ITX\_DRX\_P4\_C



## WWAN Card Conn.

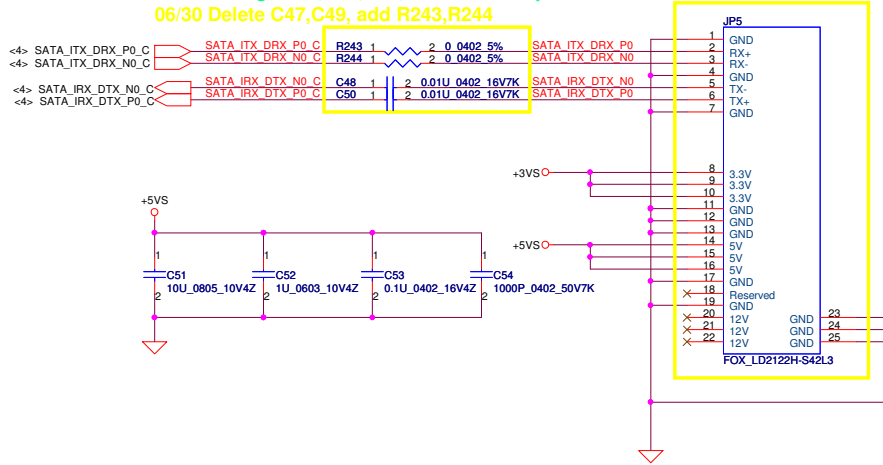


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Size	Document Number	Rev		1.0	
Custom	NTUC0 IO/B LA-5501P Schematic				
Date:	Thursday, July 30, 2009	Sheet	8	of 24	



## SATA HDD Conn.

03/24 Change C47,C48,C49,C50 from 3900pF to 0.01uF  
06/30 Delete C47,C49, add R243,R244



04/03 Change symbol (SMT connector)

05/04 Change JP5 footprint from TYCO\_1775191-1\_22P\_RV to FOX\_LD2122H-S42\_RV~D

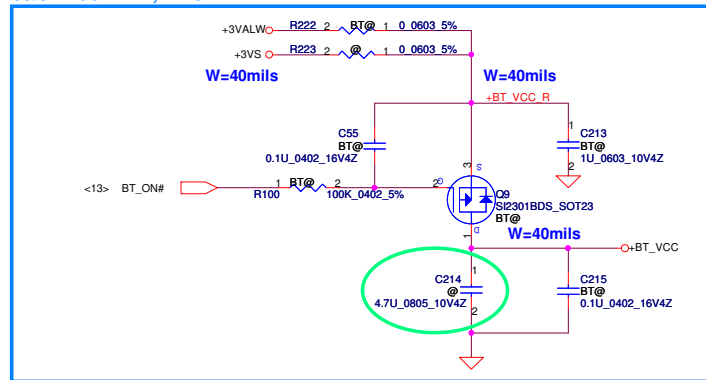
06/25 Change JP5 footprint from FOX\_LD2122H-S42\_RV~D to FOX\_LD2122H-S42L3\_22P-T

## BT MODULE Conn.

03/31 Change BT circuit (Follow NIUU1)

05/06 Change BT circuit (Follow KHLBX)

05/07 Add R222,R223

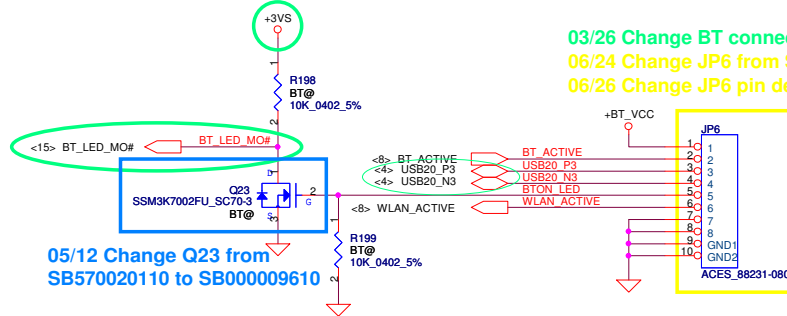


04/03 Change R198 pull-up power plane from +5VS to +3VS

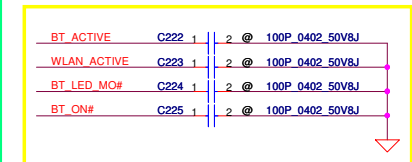
03/26 Change BT connector (Follow NIUU1)

06/24 Change JP6 from SP02000CZ00 to SP02000HC00

06/26 Change JP6 pin definition (Follow KTV00)

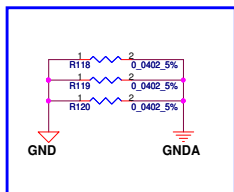
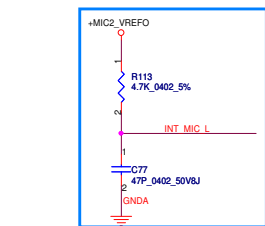
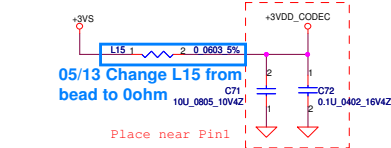
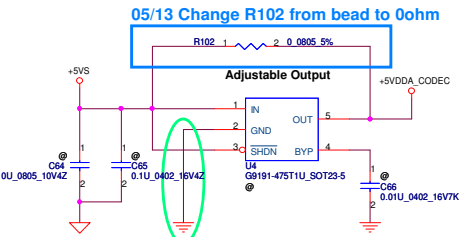


05/12 Change Q23 from SB570020110 to SB000009610

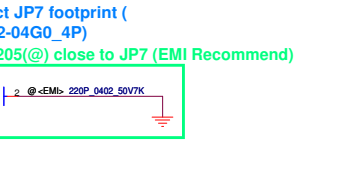
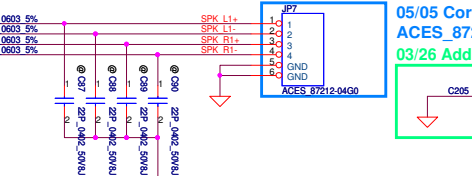
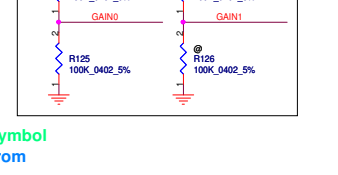
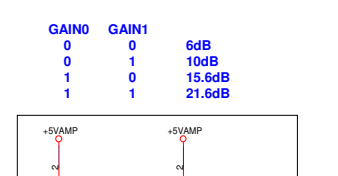
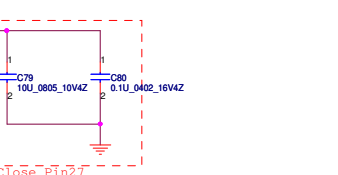
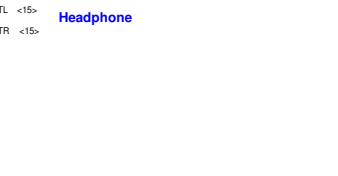
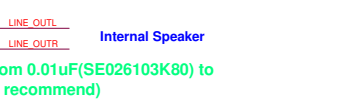
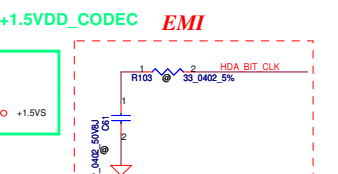
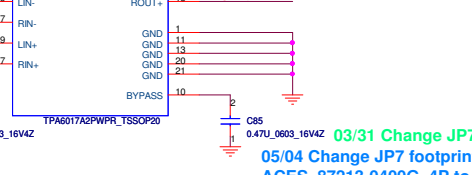
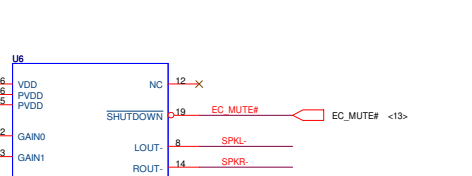
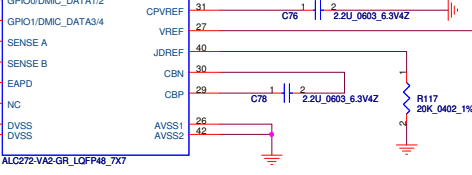
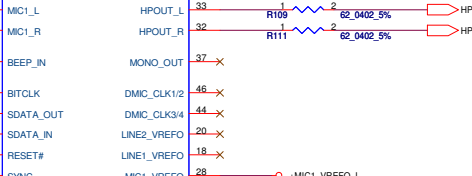
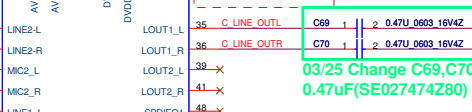
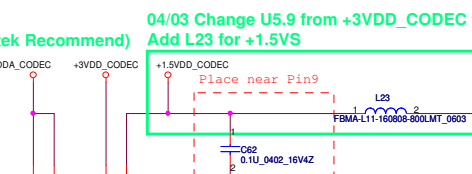
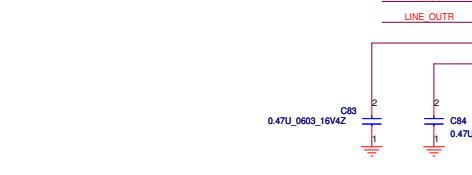
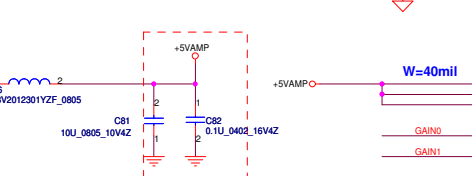
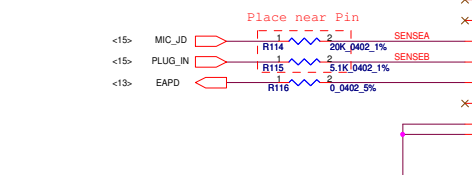
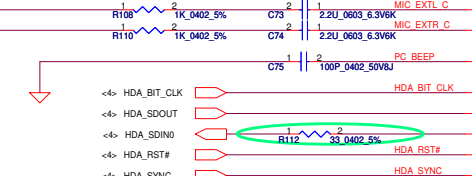
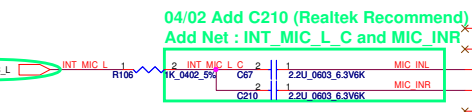
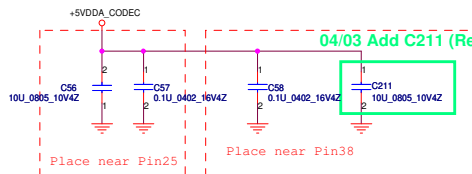
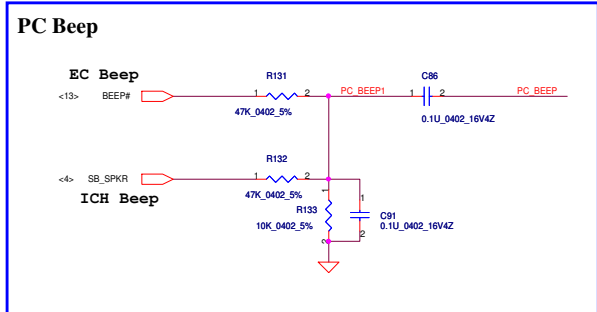


06/25 Reserve C222,C223,C224,C225 close to JP6

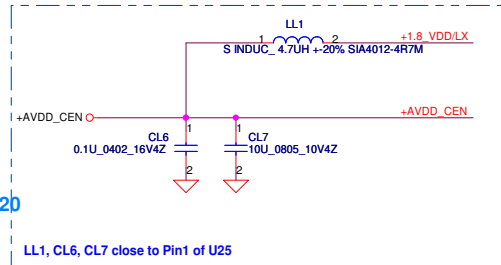
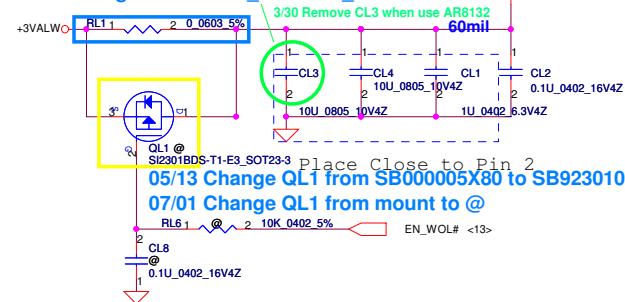
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				Date:				Thursday, July 30, 2009			
				Sheet				9 of 24			
								Rev			
								1.0			



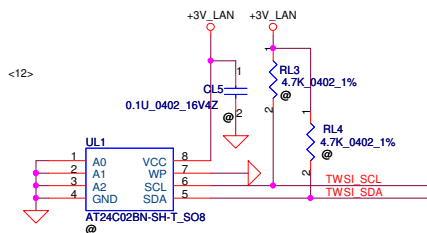
Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Mic in
MIC1 (Pin21/22)	External	Mic in
MONO-OUT (Pin37)	Internal	Internal Mic
MIC2 (Pin16/17)	Internal	Internal Mic



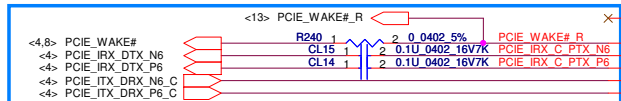
# 05/13 Change RL1 from 0\_0603 to 0\_1206



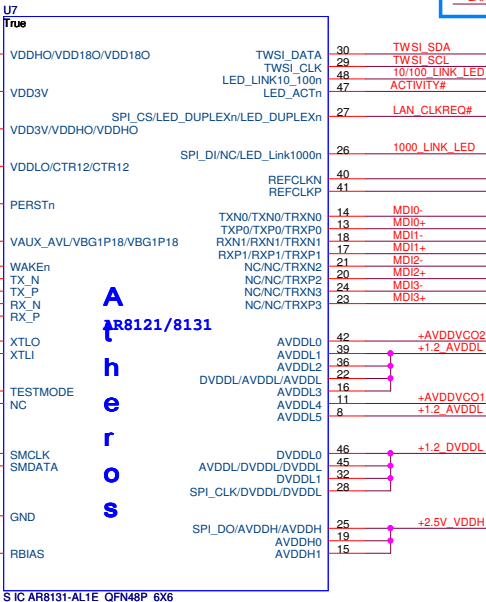
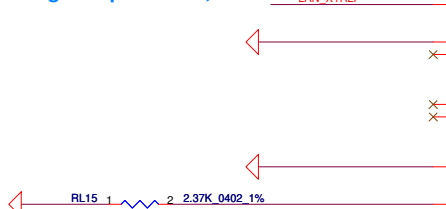
# 05/04 Add pull-up resistor RL28 for LAN.request



# 05/14 Add R240



# 04/24 Swap positive pole and negative pole of TX,RX

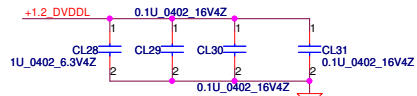


A  
h  
e  
r  
o  
s

# 02/25 Change PN of U26 from SA000038N00 to SA000031Z00

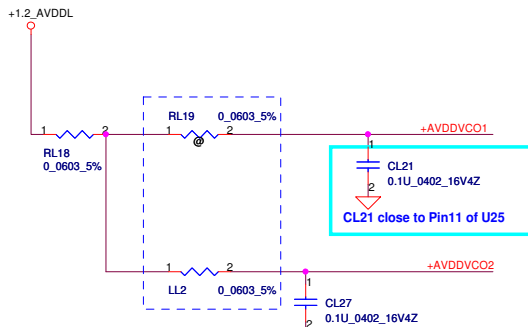
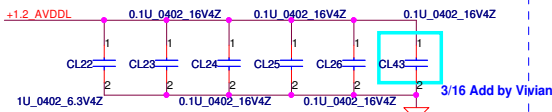
3/30 Remove U25 when use AR8132

CL28 close to Pin46, CL29, CL30, CL31 close to Pin28, Pin32, Pin45 respectively



CL24, CL25, CL26, CL43 close to Pin16, Pin22, Pin36, Pin39 of U25 respectively

CL22, CL23 close to Pin8 of U25



If overclocking, RL19, LL2 stuffed and RL18 removed.

If not overclocking, RL18, LL2 stuffed and RL19 removed.

AR8131:LL2=0ohm (more power saving mode)

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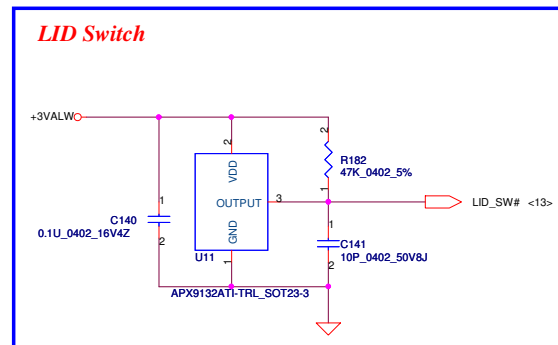
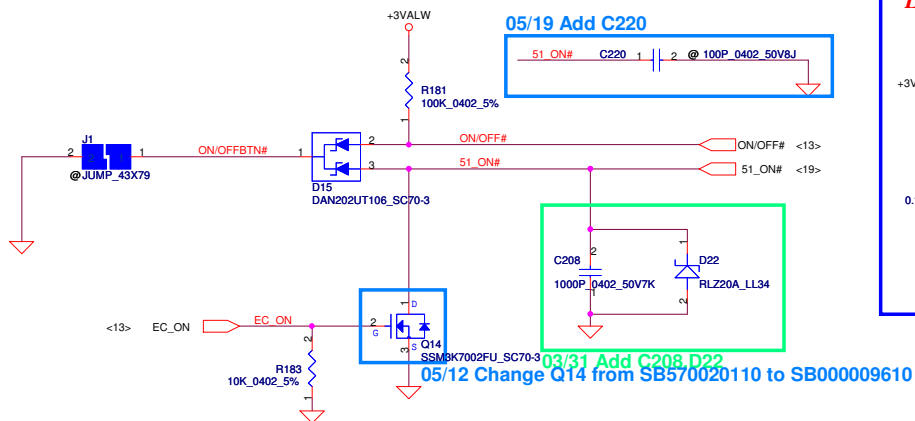


100P_0402_50V8J @ 2	1	C217	ACOFF
100P_0402_50V8J @ 2	1	C218	LID_SW#
100P_0402_50V8J @ 2	1	C219	ADP_I



### 05/04 Change R171 from @ to mount

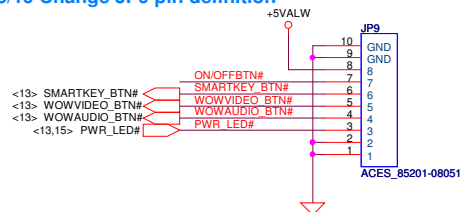
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				Size Custom	Document Number	Rev
				NTUC0 IO/B LA-5501P Schematic		
Date:	Thursday, July 30, 2009	Sheet	13 of 24			



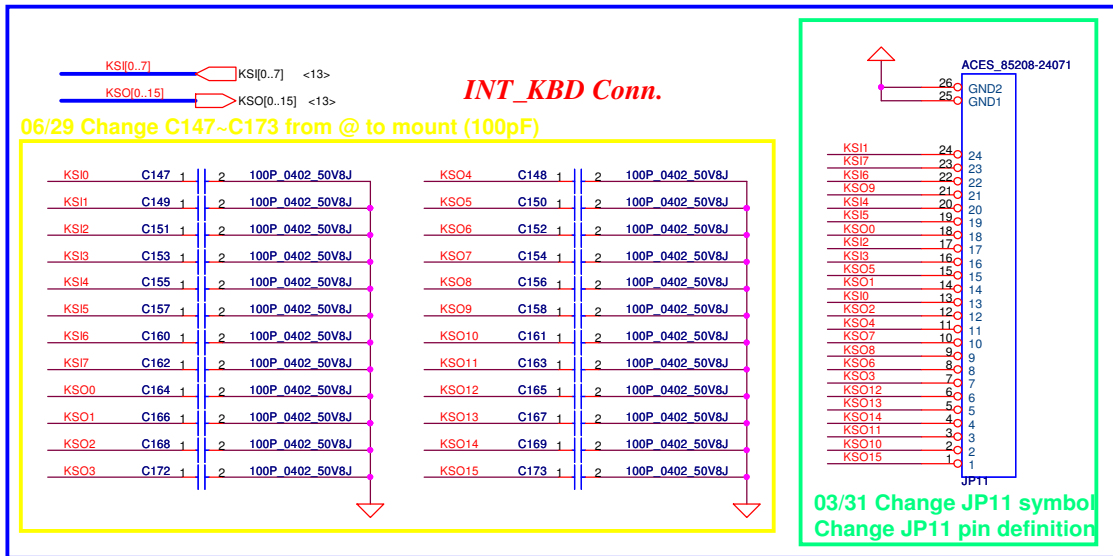
**Function BTN Conn.**

03/24 Change JP9 from 10pin to 8pin

05/19 Change JP9 pin definition



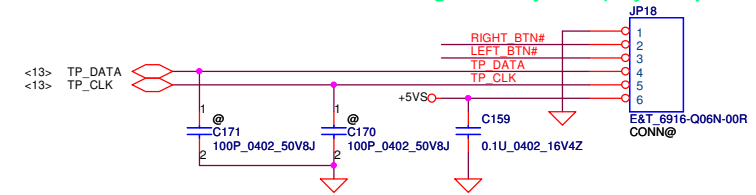
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Size	Document Number	Rev		1.0	
3	NTUC0 IO/B LA-5501P Schematic	Date:		Thursday, July 30, 2009	
Sheet		14		of 24	



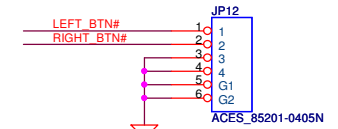
04/09 Change JP11 pin definition

To TP Module and TP/B Conn.

03/24 Add JP18 for TP module conn.  
04/01 Change JP18 symbol (Layout space limit)

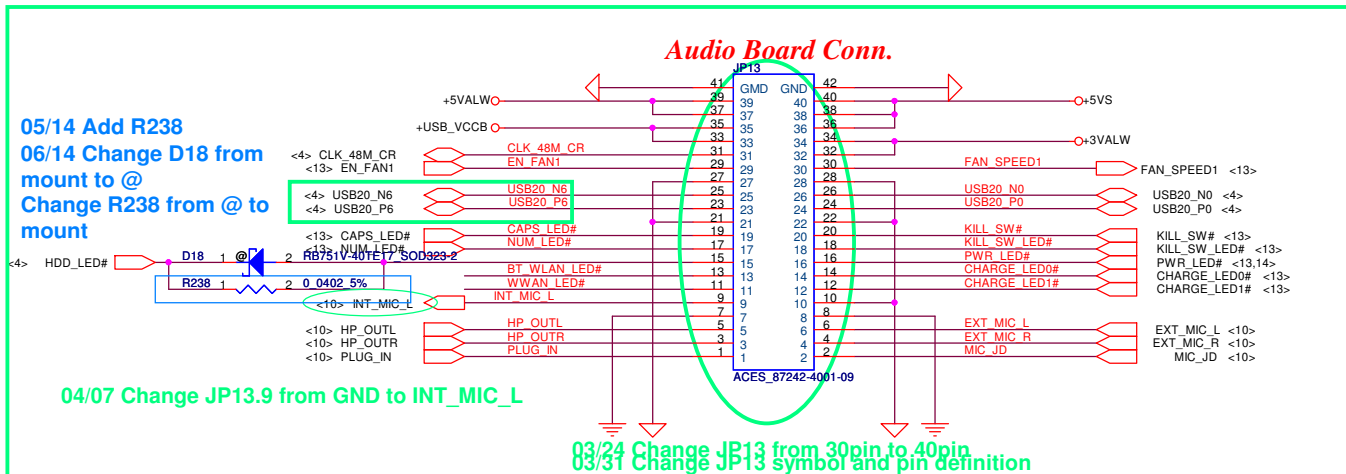
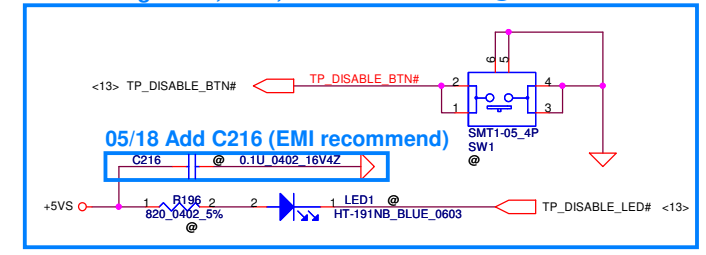


03/24 Change JP12 from TP module conn. to TP/B conn.

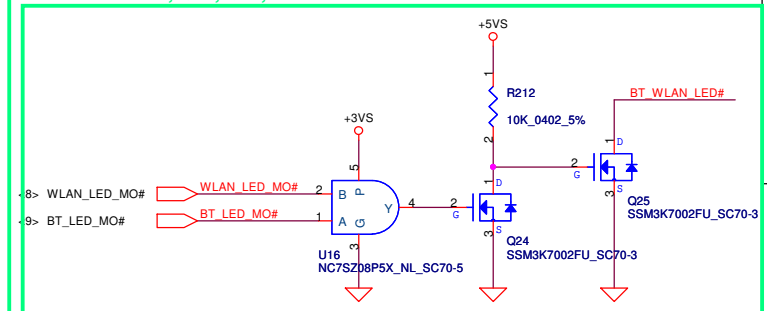


03/24 Add TP disable button and LED

05/05 Change SW1,LED1,R196 from mount to @

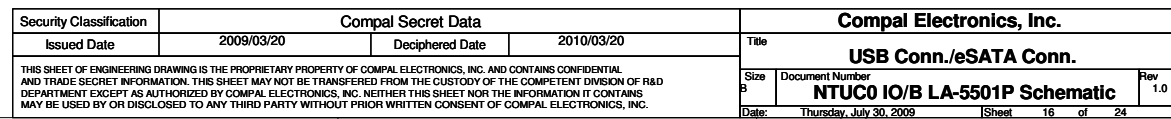
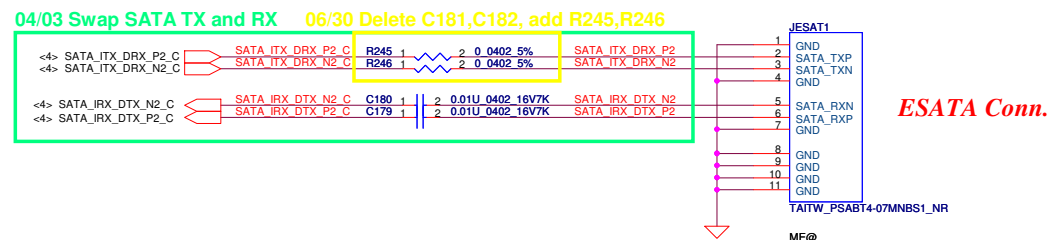


04/03 Add U16,Q24,Q25,R212



03/25 Add R200,R201 for WWAN LED

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Size	Document Number	NTUC0 IO/B LA-5501P Schematic		Rev	
3	1	Date		Thursday, July 30, 2009	
Sheet		15		of 24	



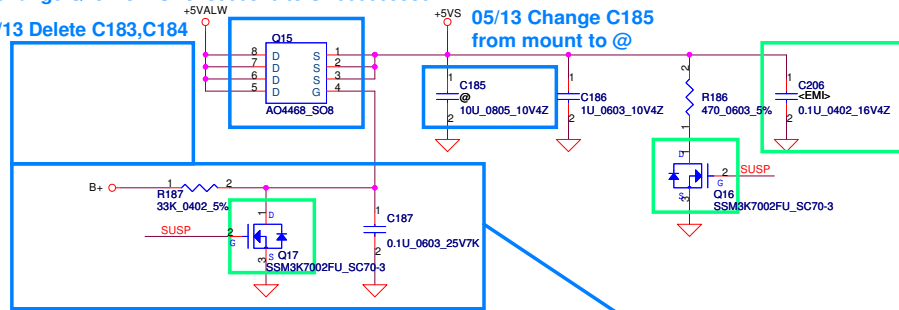


**+5VALW TO +5VS**  
**05/13 Change Q15 from SB548000310 to SB000009580**

**05/13 Delete C183,C184**

**05/13 Change C185 from mount to @**

**06/26 Add C226,C227 close to H8 (EMI Recommend)**



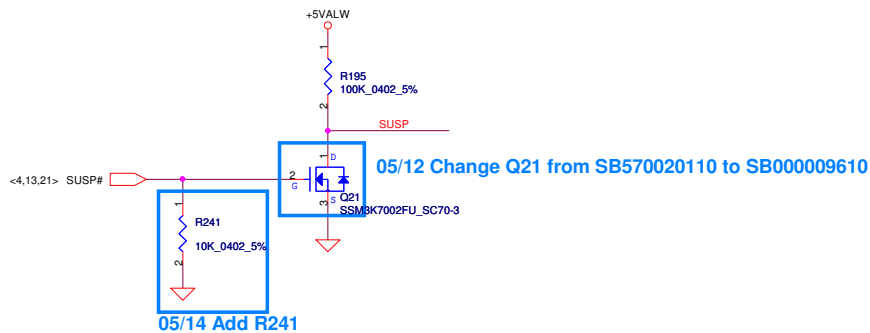
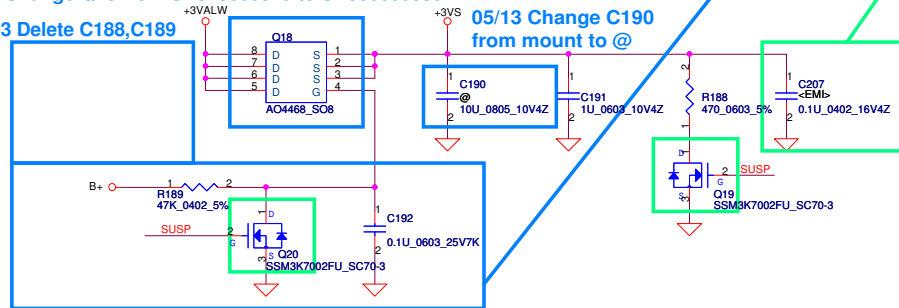
**03/30 Add C206,C207 (EMI Recommend)**

**+3VALW TO +3VS**  
**05/13 Change Q18 from SB548000310 to SB000009580**

**05/13 Delete C188,C189**

**05/13 The value of R187,C187,R189,C192 follow KHLBX**

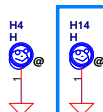
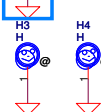
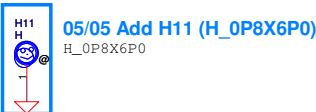
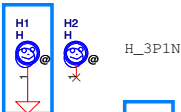
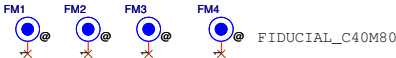
**05/13 Change C190 from mount to @**



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				Document Number	1.0
				NTUC0 IO/B LA-5501P Schematic	
				Date: Thursday, July 30, 2009	Sheet 17 of 24

05/05 Change H1 from H\_3P1X4P1N to H\_3P1X4P1

H\_3P1X4P1



05/21 Change H14 from H\_3P2 to H\_3P5



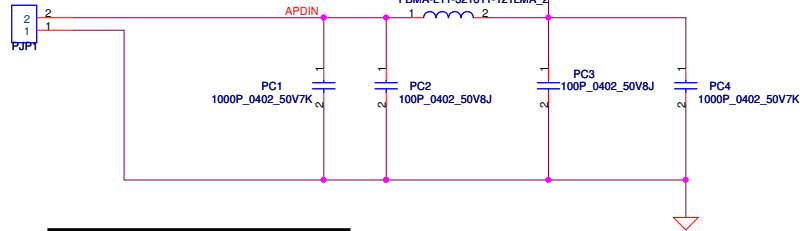
05/05 Delete H10

H\_2P8

05/12 Delete H5

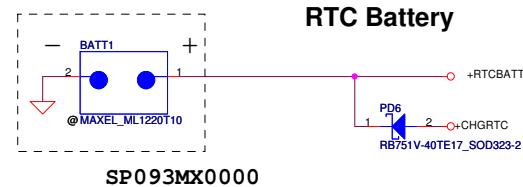
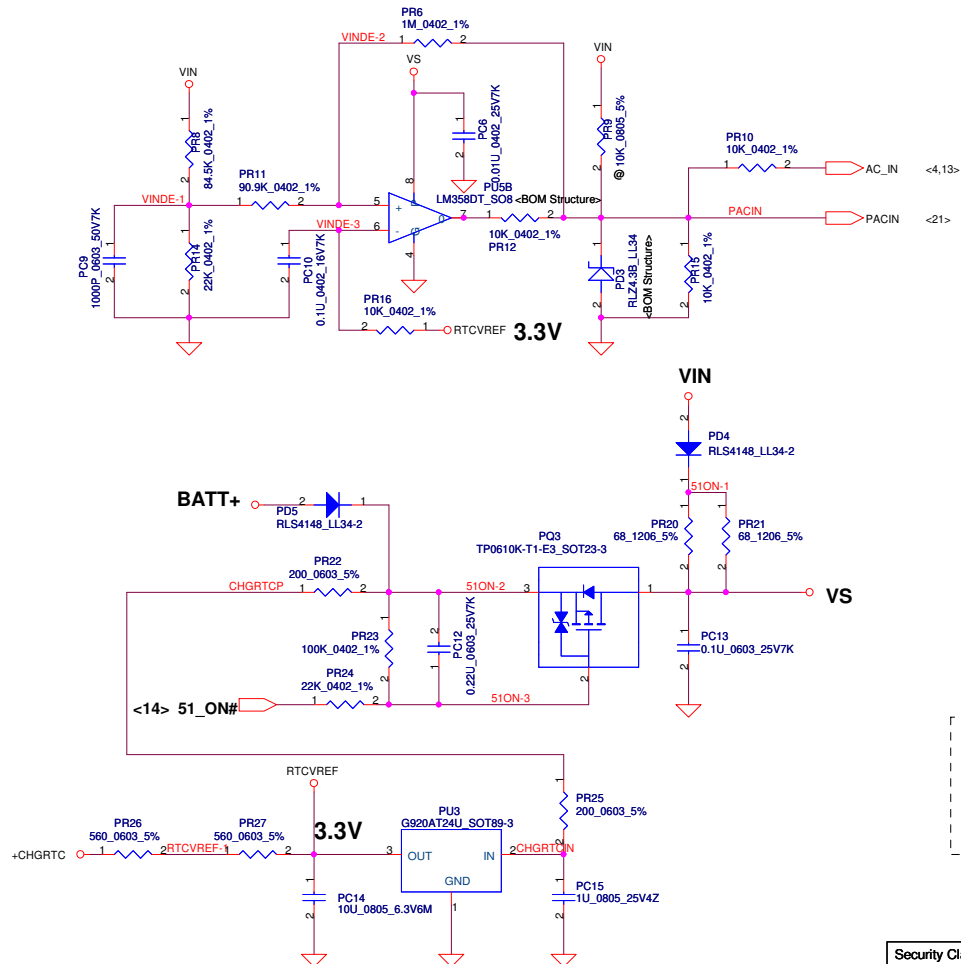
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								Size		Document Number				Rev	
								B		NTUC0 IO/B LA-5501P Schematic				1.0	
								Date:		Tuesday, July 21, 2009		Sheet		18 of 24	

@ TARNG\_TB2061HNR-02



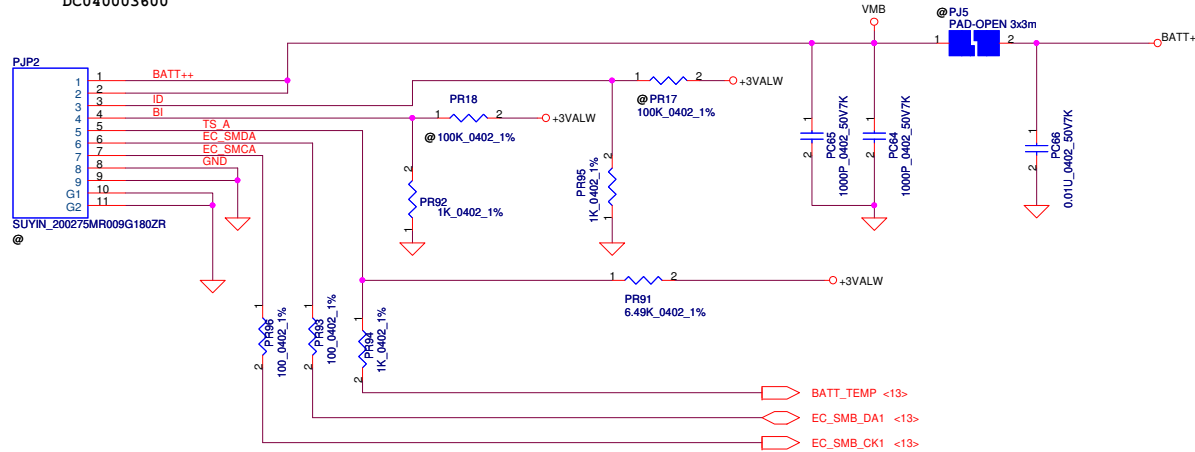
### Vin Detector

High 17.944 17.706 17.470  
Low 16.242 16.027 15.808



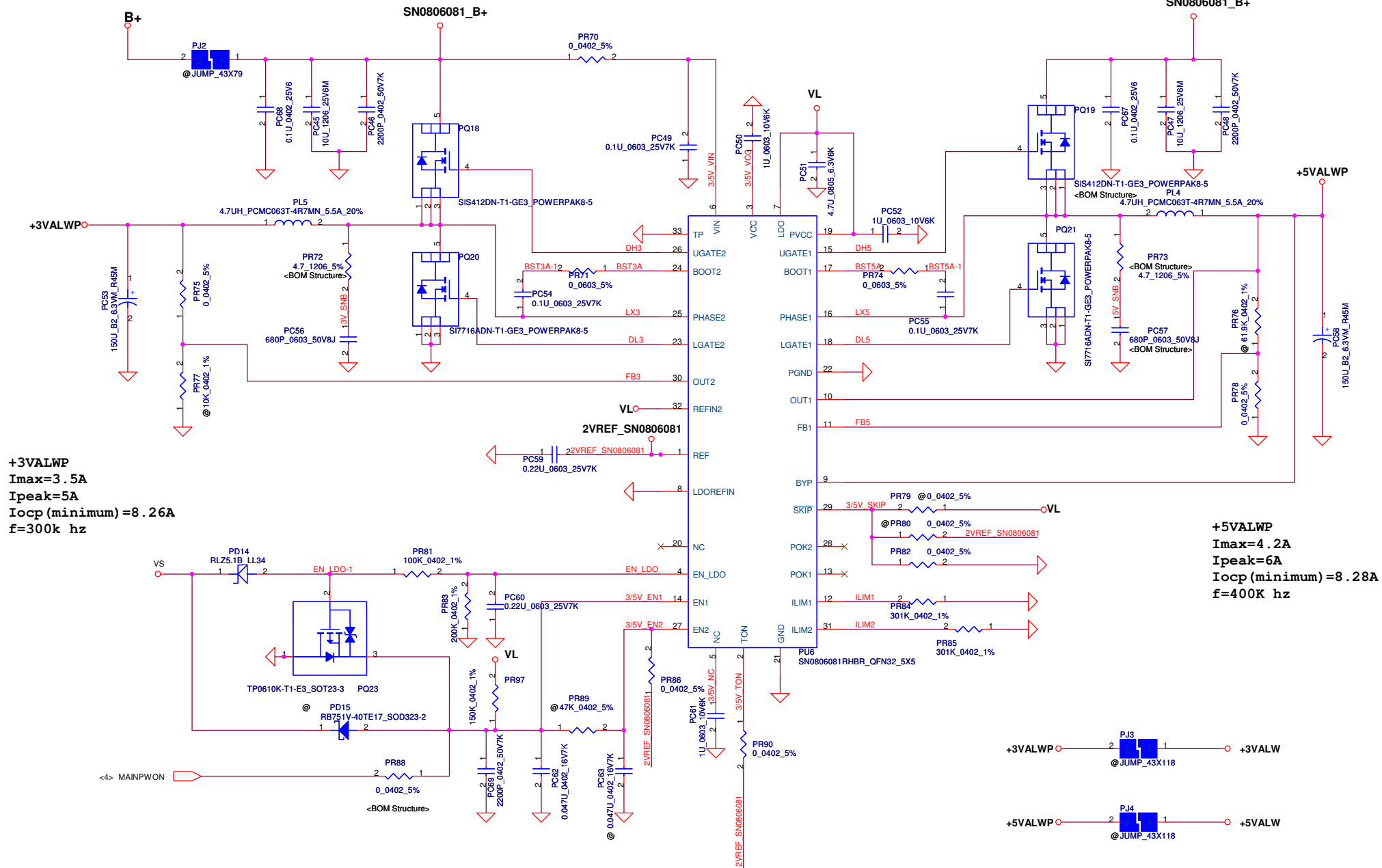
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		Custom		T				0.1	
		Date:		Thursday, July 30, 2009				Sheet 19 of 23	

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Size	Document Number	Rev		0.1	
Date:	Thursday, July 30, 2009	Sheet	20	of	23





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Size	Custom	Document Number	T	Date	Thursday, July 30, 2009
Sheet	22	of	23	Rev	0.1

## Version change list (P.I.R. List)

Page 1 of 1 for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		change CP to 2A	B		change PR58 3.48k to 0 ohm		
2		follow command design	B		Del PD13, PD15 Add PQ23		
3		PULL HIGH VL	B		Add PR97 to 150K		
4		change skip mode	B		Del PR80 Add PR82		
5		connect mainpwon	B		Add PR88		
6		RF request	B		Add PC67 PC68		
7		change charger output cap location for DFX	B		change PC38 to PC39		
8		change 50m ohm 1W current sense to 50m ohm 1/2W for 2nd source complete replace	C		change PR38 from 50m ohm 1w to 1/2w		
9		change PN form dell part to non dell part	C		change PC67,PC68 PN		
10		reduce mainpwon singal noise for hw request. Reserve PC69 space.	C		Add PC69 CAP placement		
11		reduce leakage current	C		Remove PR61	7/15	
12							
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				N PIR (PWR)	
Size		Document Number		Rev	
Custom		<Doc>		0.1	
Date:		Thursday, July 30, 2009		Sheet 23 of 23	

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
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2					
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7					
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